REMARKS

Claims 1-24 are pending in the present application. The Examiner has maintained the rejection of claims 1-7, 11-13, 17-20, and 22-24 under 35 U.S.C. §102, and of claims 8-10, 14-16, and 21 under 35 U.S.C. §103.

Section 102 Rejections

Claims 1-7, 11-13, 17-20, and 22-24 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,569,016 (Hao, *et al.*).

Applicant respectfully traverses these rejections.

Claims 1 and 12 are directed to a method and system for "aligning and inserting data elements into a first memory", and include, *inter alia*, "aligning the data element in a second memory", "dynamically generating a mask to enable writing of memory bit lines . . .", and "writing the memory bit lines to the first memory under a control of the mask, wherein said generating and writing steps are performed in response to the single store instruction". The method is "based upon an instruction sequence consisting of one or more alignment instructions and a single store instruction".

Claim 19 recites method for "storing data in a memory" that includes, *inter alia,* "aligning the data in a register relative to a location of the data within a target memory address line" and "storing a portion of the aligned data within the memory under a control of data type information and an address argument specified by the single store instruction, in response to the single store instruction". The method is "based upon an instruction sequence consisting of one or more alignment instructions and a single store instruction".

Hao is directed to a system for implementing an instruction set that can perform the functions of rotation, shifting and merging under a mask in a single machine cycle. One subset of instructions is the rotate with mask instructions. (Col. 13) In these instructions, the contents of a register are rotated a specified number of positions, and then are either inserted into another register under control of a mask provided with the instruction, or are ANDed

with the mask provided with the instruction and then placed into another register. Another subset of instructions is the rotate and store instructions. (Col. 18) In these instructions, the contents of a register are rotated a specified number of positions to generate a mask. The rotated register word is merged with the contents of another register under control of the generated mask, and are then stored in a location pointed to by the contents of another register. In some of the rotate and store instructions, an offset for the location storage is built into the instruction.

The Examiner cites two passages in Hao in rejecting independent claims 1 and 12. One of these passages discloses the rotate with mask instructions, the other the rotate and store instructions. Neither subset of instructions fully discloses the elements of claim 1 and 12. The rotate with mask instructions disclose inserting a data word from one register into another register under control of a mask provided with the instruction. This is known prior art, and is different from "writing the memory bit lines to the first memory under a control of the mask", as recited in claims 1 and 12. Note that the mask in the rotate with mask instruction is provided with the instruction, and is not dynamically generated as recited in claims 1 and 12. There is also no disclosure in Hao as to whether to the number of rotated positions is based on "aligning the data element in a second memory with respect to a predetermined position in the first memory", as recited in claims 1 and 12. In addition, there is no disclosure of "writing the memory bit lines to the first memory under the control of a mask . . . in response to the single store instruction", as recited in Applicant's claims 1 and 12.

Similarly, the rotate and store instructions merge the contents of one register into another register, this time under control of a mask generated during the instruction, before writing the data from the register to storage. Again, this is different from "aligning the data element in a second memory . . .", "dynamically generating a mask . . .", and "writing the memory bit lines to the first memory under a control of the mask", as recited in claims 1 and 12. As with the rotate with mask instruction, there is no disclosure in Hao as to whether to the number of rotated positions is based on "aligning the data element in a second memory

with respect to a predetermined position in the first memory", as recited in claims 1 and 12. In addition, the functionality of each rotate with mask instruction or each rotate and store instruction is performed during one machine instruction cycle, while Applicant's "aligning the data element . . ." is performed "in response to the one or more alignment instructions", and "dynamically generating a mask . . ." and "writing the memory bit lines to the first memory . . ." are "performed in response to the single store instruction", for a total of at least two instructions. Applicant respectfully suggests that it is the Examiner's argument that is disingenuous here.

The Examiner relies on Hao's rotate and store instruction in rejecting claim 19. The data in this instruction is rotated by a predetermined number of bits. There is no disclosure in this passage of Hao that the number of rotated positions is based on "aligning the data element . . . with respect to a predetermined position in the first memory", as recited in claim 19. Further, Hao discloses storing the full, merged word in main storage, not "storing a portion of the aligned data within the memory . . .". Applicant notes that there is no positive recitation of a merge in claim 19. Applicant urges that the Examiner's argument in paragraph 19 of the Action, that storing a full merged rotated or aligned word into memory is the same as storing a portion of a word into memory, is disingenuous. In addition, the rotate and store disclosed in Hao is a single instruction, which is different from "one or more alignment instructions and a single store instruction", as recited in claim 19.

Thus, Hao fails to disclose, teach or suggest "aligning the data element in a second memory with respect to a predetermined position in the first memory, in response to the one or more alignment instructions", "dynamically generating a mask to enable writing of memory bit lines that correspond to the aligned data element", or "writing the memory bit lines to the first memory under a control of the mask, wherein said generating and writing steps are performed in response to the single store instruction", as recited in Applicant's claim 1 and 12. Therefore, Applicant urges that Hao does not anticipate claims 1 and 12. Similarly, Hao fails to disclose, teach or suggest "aligning the data in a register relative to a location of the data within a target memory address line" or "storing a portion of the aligned

data within the memory under a control of data type information and an address argument", as recited in Applicant's claim 19. Therefore, Applicant urges that Hao does not anticipate claim 19. Reconsideration and withdrawal of these section 102 rejections are respectfully requested.

With regard to the arguments presented by the Examiner in paragraph 18 of the Action, Applicant urges that it is the Examiner's arguments of paragraph 3 of the Action that are conclusory. Claims 1 and 12 recite "aligning the data in a register relative to a location of the data within a target memory address line", and the Examiner asserts that this limitation is taught by the rotate with mask instruction and by the rotate and store instruction. Applicant urges that Hao does not teach or suggest how the number of bit positions to be rotated is determined, and the Examiner has not shown otherwise. Further, Applicant urges that the claims and embodiments described starting on page 23 of the specification satisfy the enablement and definiteness requirements of 35 U.S.C. §112, first and second paragraphs, respectively, and that no further explanation of the claim limitations is required at this time.

Claims 2-7, 11, 13, 17-18, 20, and 22-24 all depend from claims 1, 12 or 19, and are thus patentable for at least the same reasons as claims 1, 12 and 19. Reconsideration and withdrawal of these rejections are respectfully requested.

Claims 3-5, 7, 11, and 22-24 are patentable for additional reasons.

Regarding claim 3, the Examiner cites col. 13, which describes the rotate with mask instruction, and col. 18, which describes the rotate and store instructions, as disclosing computing a mask from an address argument. However, there is no disclosure in Hao's col. 13 regarding how the mask is computed, as all that is stated is that the mask is provided as part of the instruction. Therefore, Hao's rotate with mask instruction does not disclose, teach or suggest "computing a mask from an address argument", as recited in claim 3. Regarding Hao's col. 18, Applicant notes that the byte marks cited by the Examiner as being used as a mask are distinct from the mask generated by the rotate and store instruction. Applicant notes that the mask recited in claim 3 incorporates the elements of the mask of claim 1,

which recites "dynamically generating a mask". The byte marks disclosed in Hao's col. 18 are not dynamically generated by the instruction but in fact are pre-existing, and thus do not disclose, teach or suggest "dynamically generating a mask" as recited in Applicant's claim 1, or "computing the mask from an address argument" as recited in claim 3. By citing unrelated bits and pieces of Hao's disclosure to produce Applicant's invention, the Examiner is benefiting from improper hindsight gained from Applicant's disclosure.

With regard to claims 4 and 22, the Examiner states that Hao's rotate and store with update instruction discloses an address argument with a displacement value and an address value. Applicant notes that the instruction does not have an address with a displacement value as an argument, but rather the instruction has a built-in auto-pre-increment that is a part of the supporting hardware. Once again, the Examiner is benefiting from improper hindsight gained from Applicant's disclosure.

With regard to claims 5 and 23, the passage of Hao cited by the examiner (Col. 13, lines 38-39) refers to an address specified for a rotate instruction, whereas the address value recited in claims 5 and 23 are for a store instruction.

With regard to claim 7, the passage in Hao (col. 20, lines 36-40) cited by the Examiner describe a single instruction performing an entire rotate, combine, and insert in a single step. The invention recited in Applicant's claims are directed to a sequence of at least two instructions.

With regard to claims 11 and 24, column 18 of Hao discloses merging the rotated word with the word in another register under control of the mask, and storing the merged word. Thus, contrary to the Examiner's statement in paragraph 12 of the Action, the rotate and store instruction includes a merge operation, contrary to Applicant's recitation in claims 11 and 24 of "wherein the instruction sequence is without a merge instruction". Again, the Examiner is using improper hindsight gained from Applicant's disclosure to interpret Hao's disclosure, for here the Examiner stated that a merge operation that is part of an instruction (in this case a rotate and store) does not constitute being a merge instruction. The

Examiner's arguments are also inconsistent, as previously, the Examiner has stated that a rotate and store instruction was a store instruction, or that a that rotate and insert with mask instruction was an alignment instruction, even though it is an alignment and merge into register instruction.

Section 103 Rejections

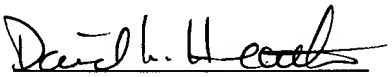
Claims 8-9 and 14-15 were rejected under 35 U.S.C. §103 as being obvious over Hao in view of Applicant's Admitted Prior Art (AAPA). Claims 8-9 depend from claim 1, and claims 14-15 depends from claim 12. AAPA was cited for disclosing a data parity and ECC. However, as stated above, Hao does not disclose, teach or suggest "aligning the data element in a second memory with respect to a predetermined position in the first memory", "dynamically generating a mask to enable writing of memory bit lines that correspond to the aligned data element", or "writing the memory bit lines to the first memory under a control of the mask", as recited in Applicant's claim 1 and 12, and the AAPA does not remedy these defects in Hao. Thus, Applicant urges that a *prima facie* case of obviousness of claims 8-9 and 14-15 over Hao and AAPA cannot be maintained. Reconsideration and withdrawal of these rejections are respectfully requested.

Claims 10, 16, and 21 were rejected under 35 U.S.C. §103 as being obvious over Hao in view of U.S. Patent No. 6,167,509 (Sites, *et al.*). Claim 10 depends from claim 1, claim 16 depends from claim 12, and claim 21 depends from claim 19. Sites was cited for disclosing the use of a read-write buffer. However, as stated above, Hao fails to teach or suggest "aligning the data element in a second memory with respect to a predetermined position in the first memory", as recited in Applicant's claim 1 and 12, or "aligning the data in a register relative to a location of the data within a target memory address line" or "storing a portion of the aligned data within the memory", as claimed in claim 19, and Sites does not remedy these defects in Hao. Thus, Applicant urges that a *prima facie* case of obviousness of claims 10, 16, and 21 over Hao and Sites cannot be maintained. Reconsideration and withdrawal of these rejections are respectfully requested.

CONCLUSION

Applicant urges that claims 1-24 are in condition for allowance for at least the reasons stated. Early and favorable action on this case is respectfully requested.

Respectfully submitted,

By: 

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